research papers

Study of radiation damage induced by 12 keV X-rays in MOS structures built on high-resistivity *n*-type silicon

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Imaging experiments at the European X-ray Free Electron Laser (XFEL) require silicon pixel sensors with extraordinary performance specifications: doses of up to 1 GGy of 12 keV photons, up to 10^5 12 keV photons per 200 μm × 200 μm pixel arriving within less than 100 fs, and a time interval between XFEL pulses of 220 ns. To address these challenges, in particular the question of radiation damage, the properties of the SiO_2 layer and of the $Si–SiO_2$ interface, using MOS (metal-oxide-semiconductor) capacitors manufactured on high-resistivity *n*-type silicon irradiated to X-ray doses between 10 kGy and 1 GGy, have been studied. Measurements of capacitance/conductance–voltage (C/G–V) at different frequencies, as well as of thermal dielectric relaxation current (TDRC), have been performed. The data can be described by a dose-dependent oxide charge density and three dominant radiation-induced interface states with Gaussian-like energy distributions in the silicon band gap. It is found that the densities of the fixed oxide charges and of the three interface states increase up to dose values of approximately 10 MGy and then saturate or even decrease. The shapes and the frequency dependences of the C/G–V measurements can be quantitatively described by a simple model using the parameters extracted from the TDRC measurements.

Keywords: XFEL; radiation damage; fixed oxide charge density; interface trap density; TDRC; C/G–V.

1. Introduction

The European X-ray Free Electron Laser (XFEL), planned to be operational in 2015, will provide fully coherent, shorter than 100 fs-long X-ray pulses, each with up to 10^{12} 12 keV photons. For its scientific potential we refer to Chapman *et al.* (2007), Murnane & Miao (2009) and the XFEL webpage (http://www.xfel.eu/research/possibilities/). The high brilliance of the XFEL poses unprecedented requirements for the detection systems: a dynamic range from single 12 keV photons to 10^5 photons deposited in less than 100 fs, a time between XFEL pulses of 220 ns, and radiation doses up to 1 GGy for three years of operation (Graafsma, 2009). To optimize sensors for these requirements demands a good understanding of the radiation damage caused by X-rays.

In this work, MOS (metal-oxide-semiconductor) capacitors manufactured on high-resistivity *n*-type silicon were used to experimentally determine the parameters needed to understand and to simulate the performance of segmented silicon sensors as a function of the X-ray dose; these are, in particular, the densities and properties of the Si–SiO$_2$ interface states and

the oxide charge density N_{ox}. Both significantly influence the performance of segmented silicon sensors, like dark current, breakdown voltage, as well as the formation of an accumulation layer below the SiO$_2$, which may cause changes in the inter-pixel capacitance, the inter-pixel resistance (Wuestenfeld, 2001) and the charge collection.

The maximum energy transfer to silicon atoms for 12 keV photons is 0.011 eV, which is well below the damage threshold of 21 eV for silicon (Akkerman *et al.*, 2001). Thus, no bulk damage is expected for 12 keV photons. The situation is different for the insulator: the band gap of SiO$_2$ is 8.8 eV (Nicollian & Brews, 1982), which is the energy required to break a Si—O bond. The average energy to produce an electron–hole pair is 18 eV (Ausman & McLean, 1975; Benedetto & Boesch, 1986). Some of the charge carriers produced by the 12 keV photons recombine. Those remaining either reach the aluminium on top of the oxide or the Si–SiO$_2$ interface. Once holes come close to the Si–SiO$_2$ interface, a fraction of them will be trapped in the oxide close to the interface, and produce radiation-induced positive fixed oxide charges (Nicollian & Brews, 1982). The fraction of electron–

hole pairs which escape recombination depends on the energy of the photons and on the field in the oxide during irradiation. In addition, interface traps are produced, which have energy levels distributed throughout the silicon band gap and whose occupation therefore changes with gate voltage. In the case of a second insulator layer, *e.g.* Si_3N_4, on top of the SiO_2, the above model has to be extended in such a way that an additional charge layer, which can be positively or negatively charged, builds up at the interface of the two insulators (Holmes-Siedle & Adams, 2002).

2. Experiments and analysis techniques

2.1. Test structures

The MOS capacitors studied were fabricated by CiS (CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Erfurt, Germany; http://www.cismst.org/) on 280 ± 10 μm *n*-doped ⟨100⟩ substrates of 5–6 kΩ cm resistivity (as determined from the C–V curve of a close-by pad diode). The insulator was made of 350 nm SiO_2 covered by 50 nm Si_3N_4. The area of the ∼1 μm-thick aluminium contact was $A = 1.767 \times 10^{-2}$ cm². To check the dependence on crystal orientation, some measurements were also performed on MOS capacitors fabricated on a crystal with ⟨111⟩ orientation.

2.2. Irradiations

For the irradiations an X-ray irradiation facility has been set up (Perrey, 2011) at DORIS, DESY. A 'white' photon beam from a DORIS bending magnet (beamline F4) was used. The maximum flux was at 12 keV and the full width of the energy spread was about 10 keV. The dose rate was calibrated by the photocurrent in a silicon pad diode. The results agree to better than 20% with calculations using the beam current, the field of the bending magnet and the geometry of the set-up. The doses quoted in this manuscript refer to the surface dose in SiO_2. The nominal dose rate of the irradiation set-up was 180 kGy s⁻¹. This dose rate could be reduced by a chopper by up to a factor of 200. For the experiments performed in this study the dose rate was about 18 kGy s⁻¹, except for the irradiations to 12 kGy and to 1 GGy when dose rates of 1.3 kGy s⁻¹ and 180 kGy s⁻¹ (full dose rate), respectively, were used. The test structures were mounted on an alumina substrate. The temperature during irradiation was typically 298 K for the reduced dose rates and 308 K for the full dose rate. It has been verified that to within 20% the results obtained did not strongly depend on the dose rate (Perrey, 2011).

2.3. Measurement and analysis techniques

The capacitance–voltage (C–V) and the conductance–voltage (G–V) measurements were made at room temperature using an Agilent E4980A bridge. An AC voltage of 50 mV and a frequency range between 1 kHz and 1 MHz were chosen.

For the determination of the parameters of the interface traps the thermal dielectric relaxation current (TDRC) technique (Simmons & Nardakarni, 1972; Mar & Simmons, 1974, 1975; Uranwala *et al.*, 1975) was used: the MOS capacitor was

cooled to 10 K biased in accumulation (0 V in our case) to fill the interface traps with electrons; then a negative voltage to bias the structure in weak inversion was applied and the sample was heated to room temperature at a constant rate of $\beta = 0.183$ K s⁻¹ while measuring the current $S(T)$ owing to the emission of trapped charges.

To extract the energy distribution and the density of interface states, the procedure of Uranwala *et al.* (1975) was used. In a MOS structure built on *n*-type silicon the relation between the temperature T and the energy E_t of a trap relative to the conduction band energy E_c is given by

$$E_t = 10^{-4}\, T\,[1.92\log(\nu/\beta) + 3.2]\,\text{eV K}^{-1} - 0.0155\,\text{eV}, \quad (1)$$

where the frequency factor is

$$\nu = N_c v_{th}\sigma_n, \quad (2)$$

N_c is the density of states in the conduction band of silicon, v_{th} is the average thermal velocity of the electrons, and σ_n is the capture cross section for electrons, for which a T^{-2} dependence is assumed (in this case the frequency factor does not depend on temperature). The capture cross section can be determined from TDRC spectra taken at different heating rates β using the method of Uranwala *et al.* (1975). We will come back to its determination later and the limitations of this method for overlapping states and states with short annealing times at room temperature.

The density of interface states $D_{it}(E_t)$ is obtained from $S(T)$ according to Mar & Simmons (1974) and Uranwala *et al.* (1975),

$$D_{it}(E_t) = \frac{S(T)}{qA\beta \times 10^{-4}[1.92\log(\nu/\beta) + 3.2]\ \text{eV K}^{-1}}, \quad (3)$$

where q is the elementary charge, and A is the area of the MOS capacitor.

As discussed later, the measurements can be approximately described by three interface states $D_{it}^j(E_t)$, $j = 1, 2, 3$. As a function of the band bending Ψ_s, assuming that charge carriers are exchanged only with the conduction band, each state j contributes to the capacitance C and the conductance G (Nicollian & Brews, 1982; Pintilie *et al.*, 2010),

$$C_{it}^j(\Psi_s) = \frac{q^2}{kT}A\int_0^{E_g} D_{it}^j(E_t)\frac{f_t^0(E_t)[1 - f_t^0(E_t)]}{[1 + \omega^2\tau_j(E_t)^2]}\,dE_t, \quad (4)$$

$$f_t^0(E_t) = \frac{1}{1 + \exp[(-E_t - q\Psi_s - q\eta)/kT]}, \quad (5a)$$

with

$$\tau_j(E_t) = \frac{1}{\sigma_n^j v_{th}N_d}\ \frac{1}{\exp(q\Psi_s/kT) + \exp[(-E_t - q\eta)/kT]}, \quad (5b)$$

$$\eta = (kT/q)\ln(N_d/N_c), \quad (5c)$$

$$G_{it}^j(\Psi_s) = \frac{q^2\omega^2}{kT} A \int_0^{E_g} D_{it}^j(E_t)\tau_j(E_t) \frac{f_t^0(E_t)[1 - f_t^0(E_t)]}{[1 + \omega^2\tau_j(E_t)^2]} \, dE_t. \tag{6}$$

σ_n^j is the electron capture cross section for state j, and N_d the doping concentration of the silicon crystal close to the Si–SiO$_2$ interface, and E_g is the band gap of silicon.

The relation between the bias voltage V_G applied at the gate and the band bending Ψ_s under steady state conditions (ignoring the 50 mV AC voltage of the capacitance bridge) is (Nicollian & Brews, 1982; Pintilie *et al.*, 2010)

$$V_G(\Psi_s) = \Psi_s - \frac{Q_{ox}}{C_{ox}} - \frac{Q_s(\Psi_s)}{C_{ox}} - \frac{\sum_{j=1}^3 Q_{it}^j(\Psi_s)}{C_{ox}}, \tag{7}$$

where Q_{ox} is the fixed charge in the isolator layer, made of SiO$_2$ and Si$_3$N$_4$ for the test structures, Q_s is the surface charge, and Q_{it}^j is the charge stored in the interface state j. Considering all interface states as acceptor-type, the charge can be expressed as (Nicollian & Brews, 1982)

$$Q_{it}^j(\Psi_s) = -qA \int_0^{E_g} D_{it}^j(E_t)f_t^0(E_t, \Psi_s) \, dE_t. \tag{8}$$

Whereas Q_s and Q_{it}^j can be calculated or determined from the TDRC measurements using the equations and references given, Q_{ox} has to be obtained from a fit of the calculated C/G–V curves to the measured ones, taking into account the voltage shift owing to Q_{it}^j. We use the equivalent circuit shown in Fig. 1 to calculate the C/G–V curves as a function of the band bending Ψ_s for different frequencies (Schroder *et al.*, 2000). C_{ox} and G_{leak} are the capacitance and conductance of the SiO$_2$–Si$_3$N$_4$ layer. From the fit of the C/V measurements to the model we find values of G_{leak} of about 10^{-9} S. The value of C_{ox}

Figure 1
Model with three interface traps used to calculate the C/G–V curves for the MOS capacitors. The symbols and the methods used to determine the parameters are described in the text.

is obtained from the capacitance measured when the MOS capacitor is biased in accumulation. C_d is the depletion capacitance of the silicon bulk below the Si–SiO$_2$ interface, which can be calculated using the Lindner approximation (Lindner, 1962; Brews, 1974). The capacitance and conductance owing to interface traps are described by C_{it}^j and G_{it}^j. The values are obtained from the TDRC measurements according to (4) and (6). C_i is the inversion capacitance owing to the minority carriers accumulated below the Si–SiO$_2$ interface, $G_r = 1/R_r$ is the sum of recombination and generation conductance owing to the traps in the depleted silicon bulk. C_i and G_r, which are only required to describe the C/G–V measurements in strong inversion for frequencies below a few kHz, are not relevant for the data discussed in this paper. $R_{bulk} = 1/G_{bulk}$ is the bulk resistance, which has to be taken into account because of the high resistivity of the non-depleted silicon. The frequency dependence of the total conductance G in accumulation allows determination of R_{bulk}. A value of ∼3.7 kΩ is found, which is about one-third of the value obtained from a naive one-dimensional model: $R_{bulk} = (\rho_{bulk}d)/A$, where d and ρ_{bulk} are the thickness and the resistivity of the non-depleted bulk, and A is the area of the aluminium on top of the isolator. The difference is not yet understood quantitatively. A three-dimensional simulation shows that the accumulation layer under the SiO$_2$ extends beyond the aluminium contact and thus the effective area relevant for R_{bulk} is significantly larger than A. For the calculation of the C/G–V curves the value of R_{bulk} determined from the measured conductance is used. For completeness, C_{bulk}, the capacitance of the non-depleted silicon bulk, is also included in the model.

From the values of Q_{it}^j, C_{it}^j and G_{it}^j obtained from the TDRC measurements as discussed above, the shapes of the C/G–V curves for different frequencies are calculated using the model shown in Fig. 1. Fixed oxide charges only shift the C/G–V curves. Thus the oxide charge Q_{ox} can be determined from the voltage shift between the measured and the calculated curves and the oxide charge density from $N_{ox} = Q_{ox}/A$. As an illustration, Fig. 2 compares the measured C/G–V curves for the MOS capacitor irradiated to 10 MGy, after annealing for 10 min at 353 K, with the result of the calculations using the optimized Q_{ox} value. It is seen that the model of Fig. 1 provides an adequate description of the data. This gives us some confidence that the extraction of the parameters is reliable.

3. Results

We first present results from MOS capacitors irradiated to eight X-ray doses in the range between 12 kGy and 1 GGy. The irradiations took between 7.5 s and 1.5 h. The C/G–V measurements were performed about 20 min after the irradiations. Owing to a significant annealing of the radiation-induced effects already at room temperature, one has to be careful with a quantitative interpretation of the data. Fig. 3 shows the C–V and G–V data for frequencies of 1 and 10 kHz. As discussed below, the voltage scans are stopped before
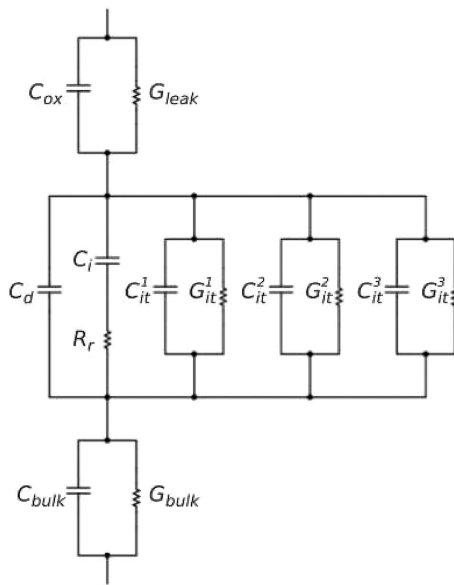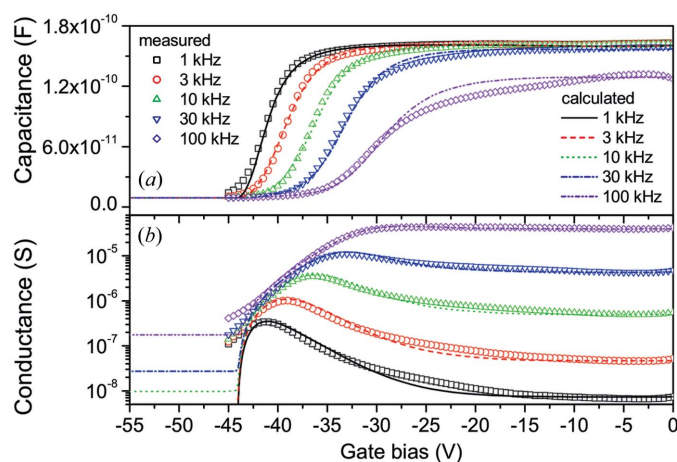
Figure 2
Comparison of the measured to the calculated C–V and G–V curves (parallel mode) of a MOS capacitor irradiated to 10 MGy (12 keV X-rays) for frequencies between 1 and 100 kHz using the model displayed in Fig. 1. (*a*) C–V curves, (*b*) G–V curves.

strong inversion is reached, to avoid the injection of holes into border traps located in the SiO_2 close to the Si–SiO$_2$ interface (Fleetwood *et al.*, 1994, 2008).
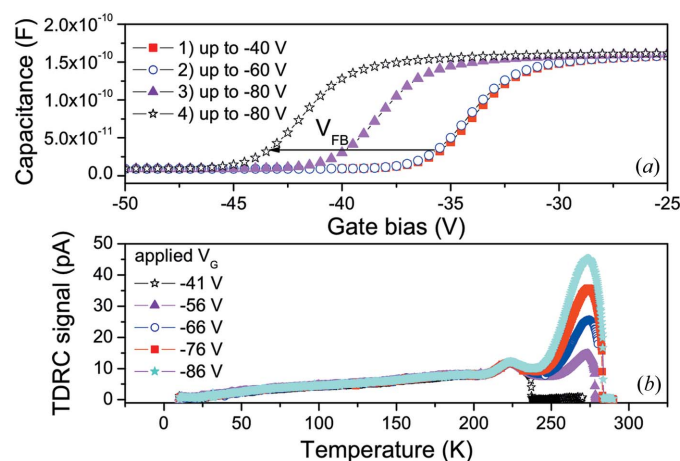
The following qualitative observations can be made. The unirradiated capacitor shows C/G–V curves close to what is expected for an ideal MOS capacitor with an oxide charge density of 1.3×10^{11} cm^{-2} (see below). The transition from accumulation to inversion occurs within ~0.5 V and only a small frequency shift owing to interface traps is seen. With irradiation the curves shift to negative voltages, the transition becomes shallower and a strong frequency shift is observed. This is clear evidence for positive oxide charges and interface traps, which can be described well by the model discussed above. The maximum voltage shift occurs for a dose of 100 MGy; the 1 GGy curves are shifted backwards by about 5 V. The reason for this is probably annealing at high dose rates during the longer irradiation time as discussed below.
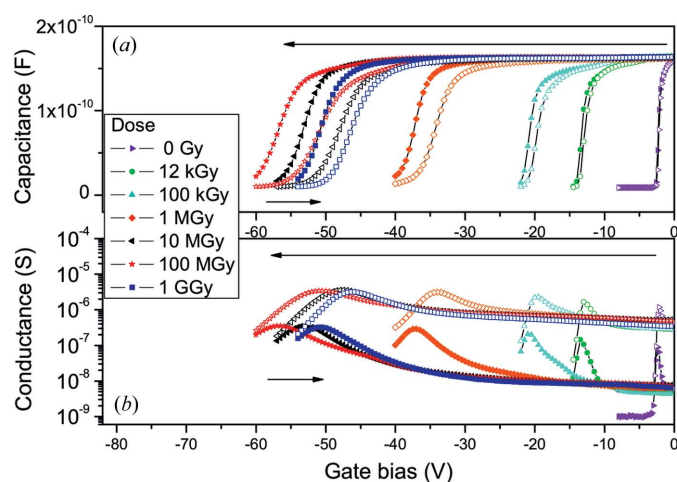
For the unirradiated capacitor the following parameters, which characterize the technology, are obtained. The constant capacitance of 163.4 ± 0.3 pF at small negative voltages, where the MOS capacitor is in accumulation, corresponds to C_{ox}, the capacitance of the SiO$_2$–Si$_3$N$_4$ layer. The value found agrees with the expectation from the area A, the SiO$_2$ and Si$_3$N$_4$ thicknesses and dielectric constants. At higher absolute voltages, where the MOS capacitor is in strong inversion, a value of 8.80 ± 0.02 pF is measured, from which an effective doping of the silicon close to the Si–SiO$_2$ interface of $6.9 \pm 1.4 \times 10^{11}$ cm^{-3} is derived. The value agrees with the bulk doping of 7×10^{11} cm^{-3} obtained from the C–V curve of a nearby pad diode. From the doping we calculate a value of $C_{FB} = 30.9$ pF for the flat-band capacitance. The flat-band voltage, V_{FB}, for the MOS capacitance before irradiation is −2.25 V, corresponding to an oxide charge density of 1.3×10^{11} cm^{-2}. This value is typical for the ⟨100⟩ orientation.

When performing the C/G–V measurements it has been observed that, for irradiated MOS capacitors biased in strong inversion, holes are injected into the border traps (Fleetwood *et al.*, 1994, 2008). They cause further shifts of the C/G–V curves. The effect is illustrated by the C–V curves shown in Fig. 4(*a*) for a MOS capacitor irradiated to 5 MGy and annealed at 353 K for 30 min. The gate voltage is cycled four times from 0 V to maximum voltages V_{max} and back to 0 V, with V_{max} values of −40, −60, −80 and −80 V. The shapes of the four curves (and their frequency dependences, not shown) are identical, but the voltages at which the flat-band capacitance is reached change. They are −36, −36, −40 and −44 V, which is evidence for additional positive oxide charges. The interpretation that the voltage shifts are due to the injection of holes into border traps when the capacitor is biased in strong inversion is confirmed in Fig. 4(*b*), where TDRC spectra for different gate voltages are shown. The TDRC signal around 270 K increases with higher negative gate voltages. It has been observed that it takes about ten days at room temperature or

Figure 3
(*a*) C–V and (*b*) G–V curves of the MOS capacitors as a function of dose (12 keV X-rays) measured at 1 kHz and 10 kHz (full and open symbols) 20 min after the irradiation.

Figure 4
(*a*) C–V curves for 1 kHz of the MOS capacitor irradiated to 5 MGy after annealing at 353 K for 30 min biased from 0 V to different maximum voltages. (*b*) The corresponding TDRC spectra. The voltage shifts and the increase of the TDRC signal are evidence for the injection of holes into the border traps, when the capacitor is biased to strong inversion.

one hour at 353 K to discharge these deep traps in irradiated MOS capacitors.

In order to obtain reproducible results and a reliable determination of the fixed oxide charge densities N_{ox}, the following procedure has been adopted: annealing of the samples for 10 min at 353 K and stopping the voltage scan before strong inversion is reached. As a criterion we use the voltage at which the measured capacitance at 1 and 100 kHz are approximately equal, as seen in Fig. 2. This procedure gives reproducible results, minimizes the effects of border charges and reduces the uncertainties owing to the short-term annealing of radiation-induced effects.

Fig. 5(a) shows the TDRC signal distribution for a MOS capacitor irradiated to 100 MGy and annealed for 10 min at 353 K. Using equations (1)–(3) the $D_{it}(E_t)$ spectrum is extracted. As shown in Fig. 5(b), its main features can be described by three states with Gaussian energy distributions D_{it}^1, D_{it}^2 and D_{it}^3 as given in Table 1. There is also a peak around 100 K which, however, as acceptor close to the conduction band, has no influence at room temperature. It should be noted here that the fit to the TDRC spectrum does not allow an unambiguous determination of the energies and widths of the different trap levels. In addition, the spectra at low

Table 1
Properties of the three dominant interface trap levels.

|	D_{it}^1	D_{it}^2	D_{it}^3
Capture cross section σ (cm^2)	1.2×10^{-15}	5.0×10^{-17}	1.0×10^{-15}
Peak energy (eV)	0.39	0.48	0.60
FWHM (eV)	0.26	0.13	0.071

temperatures change in a way which cannot be described with a single level. Thus this analysis should not be considered as an unambiguous determination of the radiation-induced interface traps but as a consistent phenomenological description of the measurements.

For the calculation of the energy distributions and of the densities of traps, the frequency factors in equations (1)–(3) have to be known for every state. They can be determined from the TDRC spectra measured for different heating rates (e.g. β_1 and β_2) following the procedure described by Uranwala et al. (1975). Thus, the frequency factor for each of the trapping centers is estimated to be

$$\nu = 10^y, \quad \text{with} \quad y = (T_2 \log \beta_2 - T_1 \log \beta_1)/(T_2 - T_1), \quad (9)$$

where T_2 and T_1 are the TDRC peak temperatures for the heating rates β_1 and β_2.

This method is only reliable if the trap levels do not overlap. However, they do, as seen in Fig. 5. In the annealing study of MOS capacitors fabricated on ⟨111⟩ silicon it has been observed that after annealing for 32 h at 353 K the signal from D_{it}^2 is significantly reduced and the signals from D_{it}^1 and D_{it}^3 are separated (Fig. 6). Thus the frequency factors for these two interface states could be determined [using equation (9)] by performing TDRC measurements with different heating rates β (between 0.1 and 0.5 K s^{-1}) after annealing for 32 h at 353 K. The estimated ranges for the frequency factors are $10^{11.6}$–10^{12} s^{-1} and $10^{11.5}$–$10^{12.5}$ s^{-1} for D_{it}^1 and D_{it}^3, respectively. These frequency factors are used in equation (2) to calculate the capture cross sections for the majority carriers at different temperatures. The values for 295 K, where C/G–V curves have
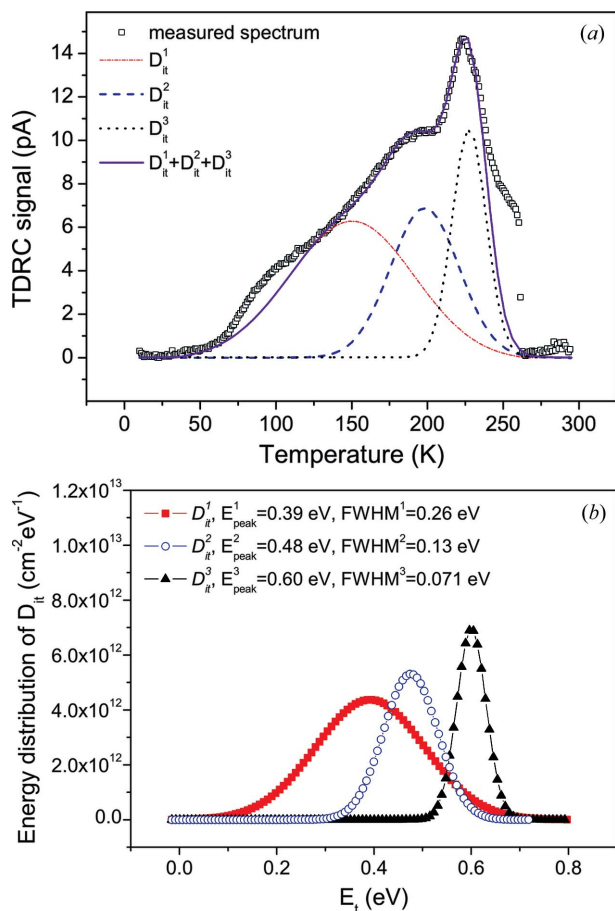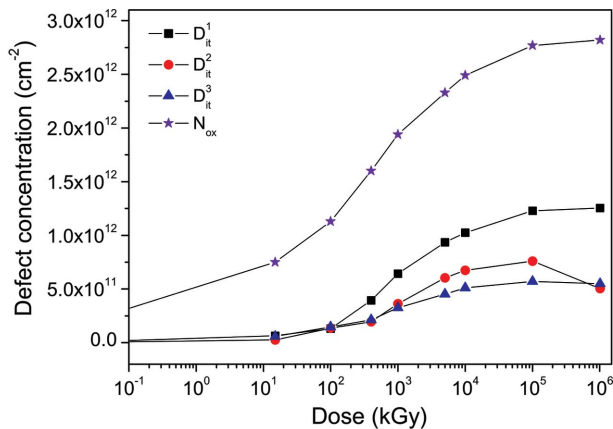

Figure 5
(a) TDRC spectrum for a MOS capacitor irradiated to 100 MGy with a fit by three dominant interface trap levels. (b) The shapes of the three dominant interface trap levels as a function of their position in the silicon band gap measured from the conduction band.
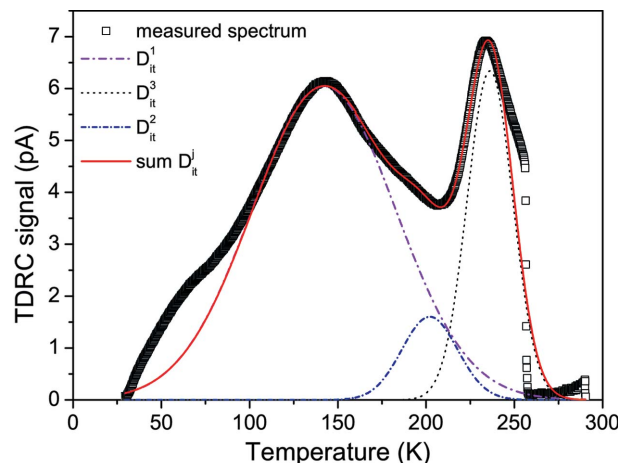
Figure 6
TDRC spectrum for a MOS capacitor fabricated on ⟨111⟩ silicon irradiated to 4.8 MGy after annealing for 32 h at 353 K. The signal owing to the D_{it}^2 state is significantly reduced owing to annealing.

Figure 7
Dose dependence of the fixed oxide charge density N_{ox} and the three dominant X-ray-induced interface states as a function of irradiation dose after annealing at 353 K for 10 min.

been measured, are given in Table 1. In the estimation the frequency shifts of the C/G–V curves have also been taken into account. With these values the capture cross section of D_{it}^2 has then been obtained by comparing the calculated C/G–V curves with the measured ones for all investigated samples after annealing for 10 min at 353 K. Table 1 summarizes the values estimated for the cross sections, the peak activation energies and the full widths at half-maximum (FWHM). When performing the annealing studies on the $\langle 100 \rangle$ crystals it has been noticed that after annealing for 72 h at 353 K a strong D_{it}^2 signal remains. Thus the method for determining the cross sections described above cannot be used here and for that reason the $\langle 111 \rangle$ values have been used in the analysis.

Fig. 7 shows the main results of the study, *i.e.* the oxide charge density N_{ox} and the integrated interface trap densities

$$N_{it}^j = \int_0^{E_g} D_{it}^j(E_t)\, dE_t \qquad (10)$$

as a function of the 12 keV X-ray dose after 10 min annealing at 353 K. It is found that all densities saturate for doses between 10 and 100 MGy with the exception of N_{it}^2, which shows a maximum at about 100 MGy and then decreases for the 1 GGy dose. This specific behavior can possibly be explained by annealing during the long-term irradiations at the high dose rate required to achieve high doses. The irradiation may locally heat the sample and cause the annealing of N_{it}^2, which is faster than for the other states. A similar study has been performed on circular gated diodes produced on $\langle 111 \rangle$ *n*-type silicon. The same three dominant interface traps with parameters compatible with those from the $\langle 100 \rangle$ MOS capacitors can describe the data. Also the dependences of N_{ox} and of D_{it}^j on dose are similar. The values for the $\langle 111 \rangle$ material are approximately 20–30% higher than for $\langle 100 \rangle$.

4. Conclusion

Results on the densities of oxide charges and Si–SiO$_2$-interface traps in MOS capacitors built on high-ohmic $\langle 100 \rangle$ and

$\langle 111 \rangle$ *n*-type silicon as a function of the 12 keV X-ray dose up to 1 GGy have been presented. The measurement techniques used are TDRC and C/G–V for different frequencies. It is found that in order to achieve reproducible results a short annealing step at 353 K is required, and the capacitors should not be biased to strong inversion to avoid the injection of holes into border states. In addition to radiation-induced oxide charges, at least three dominant interface traps have to be used to describe the measurements. Their properties and densities as a function of X-ray dose have been determined. The oxide charge density and the trap densities saturate and for one interface state even decrease at dose values between 10 and 100 MGy. The densities of radiation-induced traps and oxide charges are approximately 20–30% higher for the $\langle 111 \rangle$ material than for the $\langle 100 \rangle$ one. The shape of the C/G–V curves can be described by a simple model with parameters derived mainly from the TDRC measurements. These parameters are presently implemented in a simulation program to check if the performance of segmented sensors as a function of X-ray dose can be described and if the results can be used to design radiation-hard silicon sensors.

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