

Development of 32-channel silicon drift detectors and digital electronics for X-ray spectroscopy

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The performance of silicon-drift-detector (SDD) arrays and digital electronics designed for X-ray absorption spectroscopy in the fluorescence excitation mode is reported. Different detectors have been manufactured and tested: two single-channel SDDs with different active areas (10 mm² and 1 cm²) and a monolithic 2 cm² SDD with eight readout anodes. The energy resolution varies between 160 and 170 eV FWHM. A new digital multi-channel shaping amplifier has been produced. Its performance is presented in comparison with that of a standard commercial shaper.

Keywords: energy-resolved detectors; silicon drift detectors; X-ray absorption spectroscopy; X-ray fluorescence; digital filtering.

1. Motivation

X-ray absorption studies on highly dilute samples require the availability of energy-resolved detectors with a large counting rate capability (Jaklevic *et al.*, 1977). This has led to the development of detector arrays with a large number of parallel channels. The most common approach is to use commercially available Ge detector arrays (Cramer *et al.*, 1988). With the development of the silicon planar technology and the invention of the silicon drift detector (Gatti & Rehak, 1984), it is now possible to produce silicon detectors featuring both large active areas and good energy resolution (Gauthier *et al.*, 1994). Using silicon as a detection material has many advantages. (i) The

planar technology allows easy manufacture of many detector channels on the same silicon substrate with very low dead spaces. (ii) It is possible to integrate the JFET directly onto the readout anode, which results in excellent energy resolution for very short shaping time (Radeka *et al.*, 1989; Pinotti *et al.*, 1993; Strüder, 1998). (iii) Owing to the large energy gap of silicon compared with germanium, cooling requirements are less demanding (typically cooling to 150 K is enough to reduce the dark current of the detector). This simplifies the design of the cryostat. (iv) Mechanical handling of the detector is simple which allows fast maintenance. (v) Silicon is less sensitive to contamination than germanium, which results in better reliability.

We present herein the performance of different SDDs designed for X-ray spectroscopy: two single-channel SDDs of respective active areas 10 mm² and 1 cm², and a monolithic 2 cm² eight-readout-anode SDD. Our final goal is to produce a 32-channel detector for X-ray absorption studies on ultra-dilute samples at the ESRF beamline ID26.

With such a large number of channels, the set-up of the data acquisition may be a real source of difficulties in operating the detector. With standard electronics, the cost would be extremely high. We decided to develop new digital filtering amplifiers. This approach allows a high degree of integration (in our case, the data acquisition for the 32 channels fits in a single C-sized VXI crate), as well as complete software control: set-up and diagnosis tools may be completely automated.

2. Design and performance of silicon drift detectors

2.1. SDD geometry

An SDD is based on the combination of two different concepts (Gatti & Rehak, 1984): (i) side depletion, which allows emptying of the N semiconductor bulk of free charge carriers through a very small N⁺ implantation (this electrode also serves as the readout anode of the detector); and (ii) transverse charge collection of the free electrons generated by a photon interacting with the detector. The latter is achieved by using a drift field imposed inside the SDD bulk by segmented P⁺ electrodes implanted on both sides. The geometry of the P⁺ electrodes, and the electrostatic potentials at which they are raised, determine the drift-field topology. In the case of X-ray detection, another constraint is to reduce as much as possible the number of P⁺ electrodes on the front of the detector. This reduces the total area of the entrance windows associated with the silicon oxide over-

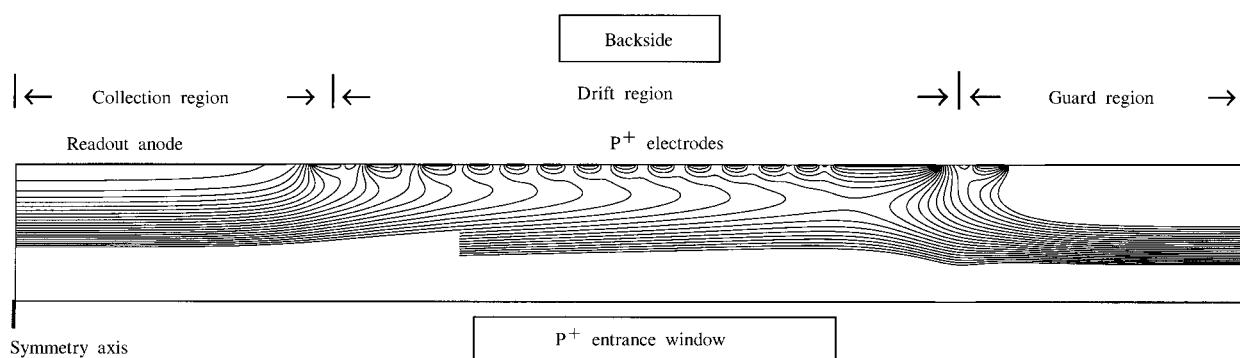


Figure 1

Cut view of a 10 mm² circular SDD. In the central part (collection region), the drift field is finely tuned in order to collect electrons towards the readout anode. In this particular case the readout anode is rather large to allow it to be glued directly to the readout JFET. In the drift region, the back consists of segmented P⁺ electrodes raised to different potentials. The outer part is the guard region. The front is a single P⁺ electrode. In the case of SDDs with a larger active area, the front electrode is segmented into two parts raised to increasing potentials.

layers insulating two adjacent electrodes. For our detectors, we have improved the field geometry that we proposed several years ago (Bertuccio *et al.*, 1992; Gauthier *et al.*, 1994): the front of the SDD is segmented into a few large P⁺ electrodes while the back is finely segmented into a large number of narrow P⁺ electrodes interconnected by an integrated voltage divider (see Fig. 1). Instead of keeping a constant voltage step between two adjacent electrodes, as was initially proposed, the geometry of the voltage divider is now finely tuned in order to keep a constant drift field inside the detector bulk. This results in a further reduction of the number of P⁺ electrodes implanted on the front of the SDD (Moguiline *et al.*, 1997).

Each of the three SDDs is circular with a thickness of 300 μm . The 10 mm² and 1 cm² SDDs each have a single central readout anode. The central part of the 2 cm² SDD is composed of eight small readout anodes surrounded by P⁺ implantations designed in order to prevent charge splitting between the anodes and cross-talk. The outer part of each SDD consists of a guard structure in order to prevent injection of high currents from the undepleted parts of the silicon wafer.

2.2. Detector and charge preamplifier assembly

The SDD is glued onto a ceramic board. The preamplifier head (a low capacitance Pentafet) is glued onto the same board near the readout anodes on a low dielectric loss insulator in order to minimize microphonic noise and stray capacitances. In the case of a single-channel SDD, the J.FET could eventually be directly glued onto the detector. A real difficulty, when working with large arrays of SDDs, is to connect, in a reliable and simple way, a very large number of wires (200 in our case) from the vacuum chamber of the cryostat to the external preamplifier boards. One has also to minimize thermal loss. We have glued flex-rigid Kapton circuits on the ceramic board. The connections to the detectors and to the J.FETs are performed using wire bonding. Multi-pin connectors are soldered onto the other end of the Kapton circuits. The vacuum feedthrough consists of a polyimide board clamped between two Viton seals. The ceramic board is screwed onto the cryostat cold finger and the multi-pin connectors are clamped onto the polyimide board. Thus, the mounting of the detector is fast and easy. A broken head can be replaced in a very short time at the synchrotron radiation facility. Another

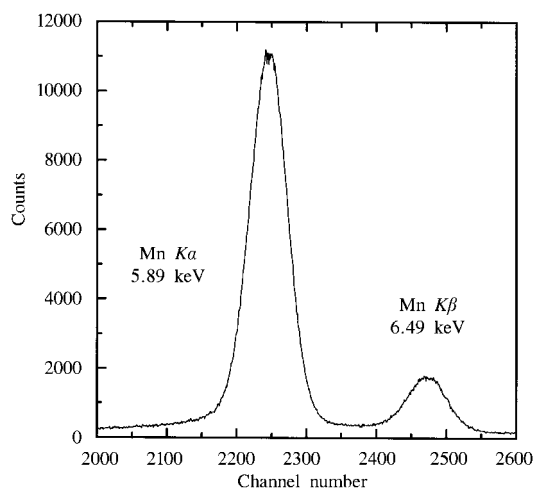


Figure 2
Typical energy resolution of the 2 cm² eight-readout-anode SDD at 150 K. The triangular peaking time is 12 μs (TC 244).

advantage of this design is that a defective component (J.FET or SDD) can be replaced without changing the other components of the detector head. This reduces maintenance costs.

2.3. Silicon-drift-chamber performance

The detectors have been tested with an analog shaper (Tennelec TC244) using triangular shaping. The best energy resolution is 160 eV FWHM at 5.940 keV (source ⁵⁵Fe) for a shaping time of 12 μs . This resolution degrades to 170 eV FWHM for an eight-readout-anode 2 cm² SDD (see Fig. 2). This is due to the larger dark current measured with this detector; we expect to improve this value by modifying the manufacturing process. The energy resolution degrades smoothly when shorter shaping times are used (230 eV FWHM at 2 μs). The energy resolution of the SDDs and the counting rates are entirely limited by the characteristics of the J.FET; it is clear that the next step to improve the performance further would be to integrate a J.FET directly onto the readout anode (Struder, 1998).

The peak-to-background ratio is 1000; we found it useful to screen the guard structure of the SDDs since the electrons created by a photon interacting in the region can be partially collected.

In the case of the eight-readout-anode SDD no cross-talk could be measured, but the peak-to-background ratio is lower (800); we believe that this is due to the long drift path of the electrons during charge collection and to residual charge splitting between the anodes.

3. Multichannel digital electronics

3.1. Digital filter design

We have developed a low-cost multichannel digital shaper in a VXI environment. Three independent digital shapers are integrated on a single C-sized VXI board. A schematic diagram of the board is reproduced in Fig. 3. Each shaper has two channels. (i) In the slow channel, the output step of the charge preamplifier is differentiated, and noise whitening is performed; a second amplifier stage is used in order to benefit from the full dynamic of the ADC. This stage includes the anti-aliasing filter. The pulse is then digitized with a 12-bit ADC running at 5 MHz. The samples are then transferred to finite-impulse-response (FIR) filters with 96 programmable coefficients, which perform the filtering. (ii) The fast channel performs a fast differentiation/amplification of the output step, then the pile-up inspector validates or inhibits

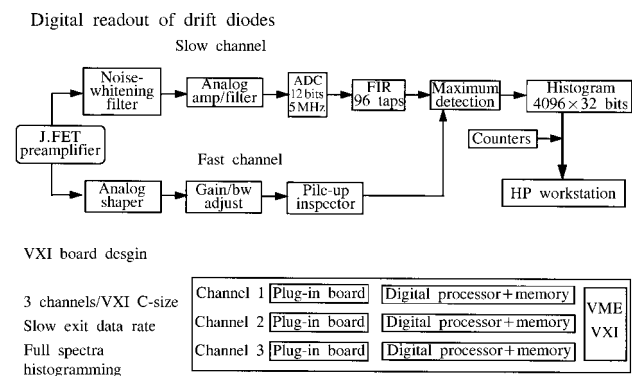


Figure 3
Functional diagram of the multichannel digital shaper. A schematic diagram of the implantation of the board is also shown.

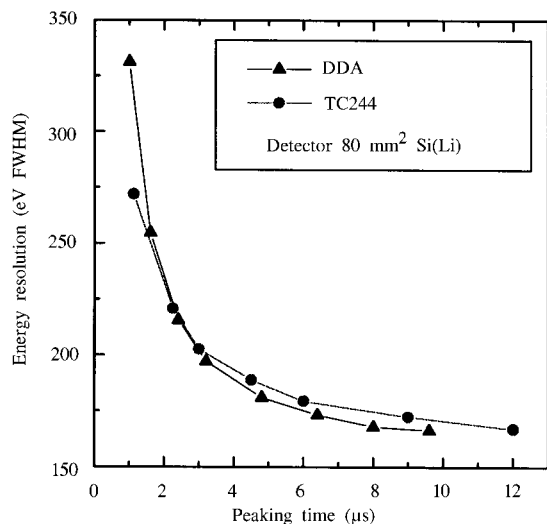


Figure 4

Comparison of the energy resolution of an Si(Li) detector measured with our digital shaper (DDA) and an analog shaper (TC244). The count rate is 2000 counts s^{-1} .

the peak maximum detection. The pulse-pair resolution of the fast channel is 400 ns. When validated, the maximum of the filtered pulse is directly histogrammed into memory buffers which are read periodically.

A very important feature not shown in the diagram has to be mentioned: the shapers perform a digital baseline restoration. Theoretically, there is no need for a baseline restorer (Jordanov & Knoll, 1994) but real detectors have defects (partial charge collection, change of dark current with photon flux *etc.*) and no perfect semiconductor is available. We believe that the implementation of a baseline restorer is mandatory if one wishes to maintain the peak position and the energy resolution when the counting rate increases.

Any kind of filter shape can be synthesized with shaping times ranging from 250 ns to 5 μs . The range of shaping times can be increased to larger values by slowing down the ADC clock, and changing the anti-aliasing filter cut-off frequency. The standard functionality of an analog system is implemented: gain setting, incident count rate, number of piled-up photons and live times are measured by different counters. An additional functionality is extremely useful: the shapers can be reconfigured into a digital-oscilloscope-type operating mode, by which digitized filtered or unfiltered pulses can be recorded, giving access to FFT analysis, filter tuning, baseline noise analysis. Since the shapers are fully controllable by computer, many operations can be automated: gain adjustment, calibration *etc.*

3.2. Performance

The digital shapers have been tested using a standard 80 mm^2 Si(Li) detector. Fig. 4 reproduces the energy resolution measured at 5.89 keV as a function of the triangular peaking time with our digital data acquisition system (DDA). We reproduce the same measurement performed with a standard analog shaper (Tennelec

TC244) and a fast ADC/MCA system (Silena ADC7423 UHS). The energy resolution achieved with the digital shaper is better for peaking times larger than 2.5 μs . For shorter shaping times, the comparison between the two systems is more complex: the analog shaper can only approximate a true triangular response. The rise times are identical but the decay time is longer with the analog shaper. For short shaping times the white noise of the J.FET is the main noise source. This noise scales as the square root of the filter length, which favors the analog shaper. We also want to emphasize that with a peaking time of 9.6 μs , we achieved an energy resolution of 166 eV, while the analog shaper only reaches this performance with a longer peaking time (24 μs). The output rate of the digital shaper is usually 10% larger (or more depending on the shaping time) than that of the analog shaper. This is related to the extra dead time introduced by the Silena ADC.

4. Conclusions

We have produced three different SDDs which achieve good performance. One 32-channel detector head comprising four 2 cm^2 eight-readout anodes has been produced and is under test. A second head made of 32 individual 10 mm^2 detectors is under production. The possibility of using these small area detectors near room temperature is under investigation. The use of digital filtering amplifiers allows reduction of the cost of the detector and improvement of the performance. This high versatility of these shapers is a major improvement with respect to the operation of a multichannel detector.

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