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A Pixel-Array Detector for Time-Resolved X-ray Diffraction

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An integrating pixel-array detector for recording time-resolved X-ray diffraction measurements on microsecond timescales has been designed and tested as a 4 × 4 pixel prototype. Operational characteristics and radiation tolerance are discussed. A 100 × 92 array with 151.2 μm square pixels is currently under construction.

Keywords: X-ray detectors; time-resolved diffraction; CMOS arrays.

1. Introduction

The development of intense synchrotron X-radiation sources has made it possible to study the time course of structural changes in macromolecules by diffraction. Knowledge of such dynamic changes in structure are potentially key to understanding many systems, including enzyme–substrate interactions, contracting muscle, and effects of stress on structural fibers of polymers and biomaterials (Gruner, 1987; Moffat, 1989; Folkhard *et al.*, 1987).

Recording time-resolved diffraction patterns requires specialized detectors. For example, charge-coupled-device (CCD) based detectors have been operated as streak cameras to record diffraction by contracting muscle (Eikenberry *et al.*, 1995). This type of detector consists typically of a terbium-activated gadolinium oxysulfide phosphor screen optically coupled to a reducing fiber-optic taper, which in turn is optically coupled to the CCD (Tate *et al.*, 1995). Impinging X-rays excite fluorescence in the phosphor and the resulting light image is captured by the CCD. A narrow slit is placed across the face of the detector parallel to the rows of the CCD to isolate the portion of the diffraction pattern to be studied, *e.g.* the equator of a fiber pattern. The vertical clock of the CCD is then run continuously during the brief exposure to X-rays of the dynamic event under study. After exposure, the clocking is stopped, and the CCD is read out normally to give the streak image. In a related clocking technique, small frames consisting of *ca* 200 raster lines are rapidly shifted into unexposed areas of the CCD for temporary storage while the other frames are exposed. After the shutter is closed, the CCD is read out normally to show the, for example, five accumulated frames. This method was used recently to record anisotropic coarsening of grooves in silicon (Yoon *et al.*, 1998).

CCD-based streak cameras have simultaneously achieved about 0.25% resolution in spacing and 1 ms resolution in time on the 10 reflection of contracting muscle, which measures the 417 Å interfilament distance in the tissue (Eikenberry *et al.*, 1995). Further improvements in the speed of this type of detector will be difficult to achieve, most especially because of phosphor lag, the delayed emission of light by the phosphor after X-ray excitation. Even phosphors that are regarded as decaying quickly frequently only do so to the 10% level, and have severe long-lasting afterglow (Shepherd *et al.*, 1995). An additional disadvantage of streak-camera techniques is that only a line or small portion of the image is recorded rather than the full two-dimensional diffraction pattern.

2. The pixel-array detector

To overcome the limitations of phosphor-based detectors and permit recording of full two-dimensional diffraction patterns on a microsecond timescale, we have designed and are constructing an all-silicon pixel-array detector (PAD) (Barna, 1997). The PAD is a two-layer device consisting of an array of X-ray sensitive photodiodes bonded to a CMOS electronics layer. The diodes, lithographically patterned as an array of pixels on 300 μm-thick high-resistivity silicon, are connected pixel-by-pixel to the electronics layer by an array of solder bumps. In operation, the diodes are fully depleted by an applied reverse bias of *ca* 60 V, which serves to collect holes and inject the resulting current into the measurement electronics associated with each pixel. Although each pixel implant region in the diode array has a 15 μm-wide border surrounding it,

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no X-rays are lost between pixels: charge deposited at the boundary between pixels is divided between them.

We chose to design an integrating detector because the predicted X-ray event rate in many diffraction applications at newer sources will be in the range of gigahertz in the peak pixels of some Bragg spots, far exceeding the capability of counting electronics. A counting-type pixel-array detector that should be useful with lower event rates is under development elsewhere (Beuville *et al.*, 1996). Each pixel in the PAD contains a charge integrator, a switched array of eight storage capacitors and an output buffer (Fig. 1). The storage capacitors associated with each pixel can be switched in parallel in *ca* 200 ns, permitting eight image frames to be captured in as little as 1 μs each, though accuracy should improve with longer integration times. After image acquisition the stored frames are read out through a single output port by row-and-column addressing.

A 4 × 4 pixel prototype of the PAD with 150 × 150 μm pixels was fabricated and tested with a laboratory X-ray source (Barna *et al.*, 1997). The CMOS layer was fabricated in a 1.2 μm process at Hewlett-Packard through the MOSIS Service (Marina Del Rey, CA, USA). A summary of the results obtained is given in Table 1.

Table 1
Results of testing the 4 × 4 pixel prototype of the PAD (Barna *et al.*, 1997).

Measurements are expressed in terms of equivalent numbers of 8 keV X-rays.

Pixel saturation capacity, X-rays	19500
Electronic noise, X-rays	4–5
Maximum average integration rate, X-rays	23000 μs^{-1}
Leakage current, X-rays	14.4 ms^{-1}
Charge collection efficiency	93%
Non-linearity	<0.2%
Point-spread amplitude at 75 μm	<1%

3. Time-resolved experiments at CHESS

Time-resolved studies using the 4 × 4 prototype were carried out at the Cornell High Energy Synchrotron Source (CHESS) using 13.6 keV radiation on beamline A-1. These experiments had the dual objectives of studying possible fluctuations in time of the intensities of Bragg spots produced by several highly solvated liquid-crystalline materials, and studying the response of the PAD to high doses of X-rays (Barna, 1997). To look for intensity fluctuations, observations were made of the both the main beam and selected sharp Bragg spots from the liquid crystal. Using various integration times with aluminium absorbers to reduce the intensity of the main beam, it was found that there was a prominent 30 Hz component along with its harmonics in all measurements that had not been observed in the laboratory measurements. This component dominated the putative fluctuations expected from the crystal and was attributed to mechanical instabilities; alternatively, the variations may be attributable in part to beam fluctuations. Interestingly, unrelated time-resolved studies using the CCD streak camera on the same beamline showed a strong *ca* 120 Hz component, which was tentatively attributed to line interference (Eikenberry *et al.*, 1995). These observations underscore the necessity of having temporally stable synchrotron beams for time-resolved studies, and show that the PAD can easily record dynamic X-ray patterns.

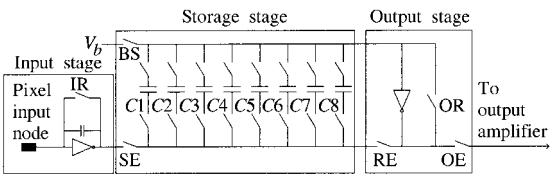

Figure 1
Schematic diagram of the CMOS electronics associated with each pixel of the PAD. The X-ray sensitive photodiode is bonded to the pixel input node. Current from the conversion of X-rays in the diode is integrated in the input stage and stored on one of the eight switched capacitors, C1–C8. The output stage buffers the stored voltage for transmission to the output. The switches shown control the various operating modes: IR, integrator reset; SE, store enable; RE, read enable; OR, output reset; OE, output enable; and BS, bias select. V_b is a bias voltage.

4. Radiation damage studies

Calculations of radiation absorption indicate, unfortunately, that for a 300 μm-thick detective diode layer, maximum damage to the CMOS electronics should occur with an X-ray energy of 13.5 keV, a commonly used energy at synchrotrons: approximately 0.5×10^6 X-rays per pixel of this energy are calculated to deposit 1 rd (1 rd = 10^{-2} Gy) in the electronic layer. It was observed during the studies of the main beam at CHESS that removing attenuation caused an increase in the measured leakage of the photodiodes. Upon further increases in dose, one of

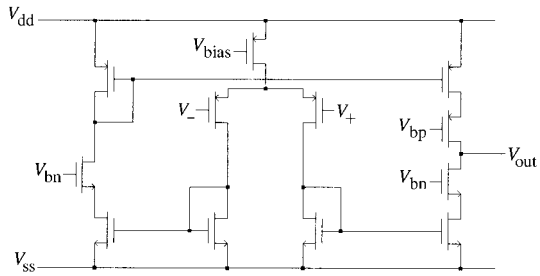

Figure 2
Schematic diagram of the differential cascode amplifier being tested for the integrator to improve the pedestal stability. V_+ and V_- represent the differential input voltages; V_{out} is the output; V_{bias}, V_{bn} and V_{bp} are bias voltages setting the operating point of the cascode circuit; and V_{dd} and V_{ss} are the supply voltages. The schematic diagram of the output-stage amplifier, shown in Fig. 1, is identical to this amplifier, but the lengths and widths of the gates are optimized differently for the two applications.

the storage cells began to respond as if negative voltage were being stored. This effect disappeared after a few days, and was attributed to oxide charging in the CMOS.

In a high-exposure test, an integrated dose calculated to be in the range 10–50 Mrd was applied to the CMOS with no power to the electronics. This is far larger than the rated radiation tolerance of standard CMOS, which is approximately 10 krd. Afterwards, the device responded as if the leakage currents were very large, even on a microsecond timescale; the dark current pedestal also increased dramatically. However, after keeping the device cool overnight, leakage reduced considerably with several pixels returning to normal operating values. Thus, the PAD in its present form is quite susceptible to radiation damage, but not all the damage is permanent and the PAD spontaneously recovers with time to some degree.

5. Design of the large-area PAD

As the next step in making a full-scale large-area detector, a 100 × 92 pixel device is in fabrication, with testing expected in the fall of 1997. Like the 4 × 4 prototype, the CMOS was fabricated in a 1.2 μm process by MOSIS. The pixel structure is slightly modified from the 4 × 4 pixel prototype by the addition of a fully cross-linked grid for the power supplies throughout the array. This change, which was made to minimize the local voltage drop in pixels subjected to very high X-ray flux, increased the pixel size to 151.2 × 151.2 μm. Thus, the active area of the PAD is 15.12 × 13.91 mm, which together with the abutting row-and-column address lines and associated switches, fully occupies the maximum die size permitted in the MOSIS program. The diode layer was fabricated by Sintef (Oslo, Norway); the solder bump-bonding was performed by GEC–Marconi (Caswell, Towcester, Northamptonshire, England).

Because the PAD chip has 145 bonding pads on four sides, most of which are parallel connections to the power supplies, standard packaging options are not applicable. Instead, the chips are epoxied to individual carriers of thermally conductive ceramic, which in turn are mounted in individual printed-circuit (PC) boards having an opening so that the cold finger of the cryostat, can contact the ceramic. The PC boards provide pads for wire bonding and have traces to distribute the power supplies and route the control signals to a pair of dual in-line connectors. Wire bonding of the chip to the carrier was performed by Promex, Inc. (Santa Clara, CA, USA). The resulting assemblies plug in easily to a larger PC board in the evacuated cryostat, which provides a light tight, temperature-controlled environment for the PAD (Barna *et al.*, 1997). The circuit board in the cryostat provides power supply decoupling and generates the three bias voltages required by the cascode structure of the PAD output amplifier.

The current realization of the PAD has a single analog output representing the stored value on a capacitor at a specified row-and-column address. Each PC chip carrier has an op-amp (AD845; Analog Devices, Norwood, MA 02062, USA) operated as a follower with a gain of 2.5 to buffer the analog output of the PAD as close to the chip as possible and to adjust the output voltage scale to match the scale of the analog-to-digital (A/D) converter. This output is connected *via* a short shielded cable to the 16-bit, 2 MHz A/D converter (ADC4322; Analogic Corporation, Wakefield, MA 01880, USA) which is housed in a separate enclosure and mounted on a custom PC board that provides shielding, isolation of digital and analog signals, and power-supply decoupling.

Although the PAD is organized physically as a 100 × 92 array of pixels, electrically it has 200 rows each with 46 columns. Thus, an 8-bit row address and a 6-bit column address must be supplied to select a pixel for readout. Together with other control lines setting the states of switches in the array, 30 digital inputs are required by the PAD. Additionally, the A/D converter has one control input and 17 digital outputs (a ready signal and 16 data lines). Thus a total of 48 digital lines and considerable random logic are needed to interface the PAD to the host controller. The control functions for the 4 × 4 prototype were readily provided by a Hewlett-Packard 16500B logic analyzer, without the need for custom logic, but the 100 × 92 array is much more complex (Barna, 1997).

It was decided to implement the PAD controller using a reconfigurable processing unit (RPU; model XC6214, Xylinx Inc., San Jose, CA 95124, USA) to provide random logic and control-signal sequencing. The hardware is provided on a PCI bus card with 512 K static RAM suitable for installation in a personal computer or workstation (Virtual Computer Corp., Reseda, CA 91335, USA). It was decided to use differential line drivers and receivers for all the control lines (48 twisted pairs), but by using the RPU approach no other logic circuits are required between the RPU board and the PAD–A/D unit. Further, the hardware can be assembled before the logic design is completed.

The RPU is configured using standard design tools so as to implement a very simple computer, with an instruction pointer and accumulator, which executes a program stored in the memory on the board (Wirth, 1995). The program in turn sequences timers, address counters, and control registers which feed digital signals to the PAD. Output from the A/D converter is accepted by the program and stored in computer memory *via* the PCI interface. The structure of this virtual computer defines a hardware language, for which a simple two-pass assembler was written in the C programming language. In operation, after the computer is powered up and the PCI interface is configured, a program configures the logic design in the RPU, after which a high-level control program can communicate with the hardware to control the PAD either on a step-by-step basis, or set up a program on the RPU board to acquire PAD images and store them in computer memory. The advantage of this approach is that the firm-

ware is easily reconfigured to perform different functions, such as operating test chips. Thus, a single hardware setup can, with only software changes, perform several distinct functions that would have required rewiring in the past.

6. Design modifications and future developments

In addition to work on the 100 × 92 PAD, some problems that appeared in the tests of the 4 × 4 prototype are being addressed in new test chips. Most serious of these was an instability in the pedestal value of the pixels, which contributed significantly to the noise in background subtracted images. This instability was attributed to the use of a single-ended amplifier for signal integration. A differential amplifier has been designed and incorporated into a test chip (Fig. 2), which has been fabricated in a 0.5 μm process by MOSIS. This smaller process was adopted both because the 1.2 μm process is being phased out and because the savings in area permit the differential amplifier to be even smaller than the previous single-ended amplifier. A key consideration regarding the adoption of the 0.5 μm process is that it has a capacitor with good linearity, a necessity for the integration and storage capacitors.

A second problem was the effect of detector noise, *ca* 4–5 X-rays per pixel, on low signals. This has been addressed by incorporating a much smaller charge-integration capacitor, and adding a gate on the previous large capacitor, thus providing on-chip gain switching through selection of the capacitance value. Another architecture to be tested is one that permits continuous simultaneous integration and readout by having switches that allow one capacitor to store charge while the other is being read. The speed of this continuous framing device is, of course, limited by readout speed. Both of these modifications and combinations thereof have been fabricated on a single chip that will be tested in the fall of 1997.

This emphasizes one of the great advantages of the PAD architecture. One can devise a pixel with new functionality, and test it easily and at low cost by having a test chip fabricated. Then, when the design is fully developed, one can simply replace the pixel in the full array, and have very high confidence that the entire unit will work as expected. One idea being explored is a device with in-pixel auto-correlation, which would permit direct study of the statistics of X-ray fluctuations over a wide range of time-scales.

A third problem observed in the prototype was the susceptibility to radiation damage. Several approaches are under consideration to mitigate this problem. One approach is the adoption of a radiation-hard CMOS process. Several vendors now offer such processes to commercial users, and they are reputed to be reliable at radiation doses of several Mrd.

Another approach is the introduction of a radiation-blocking layer between the diodes and the CMOS layer. A proposed design for such a layer consists of a 1 mm-thick leaded-glass capillary plate with a high-Z metal filling the vias to establish electrical connection between the diode and CMOS layers. Though this design entails several engineering challenges, it offers the most thorough solution to the problem of radiation damage.

A third approach is the use of GaAs to fabricate the diode layer, which would provide considerable shielding because of its high atomic number. GaAs, however, has the considerable disadvantage of having much higher dark current than Si. However, recent studies indicate that this current can be reduced greatly by cooling to 233 K. To test this approach, diode arrays are currently being fabricated at the University of Sheffield on 200 μm thick GaAs material, and are expected to be tested in the fall of 1997.

Because silicon fabrication is relatively low cost in large quantity, the PAD has the potential to be a relatively inexpensive X-ray detector once it is fully developed. Large-area detectors should be possible by tiling chips, perhaps overlapping them like shingles. Coupled with the flexibility inherent in the pixel design, the PAD appears to be a promising technology.

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